

FIG 1A

NMOS transistor

NPN bipolar transistor

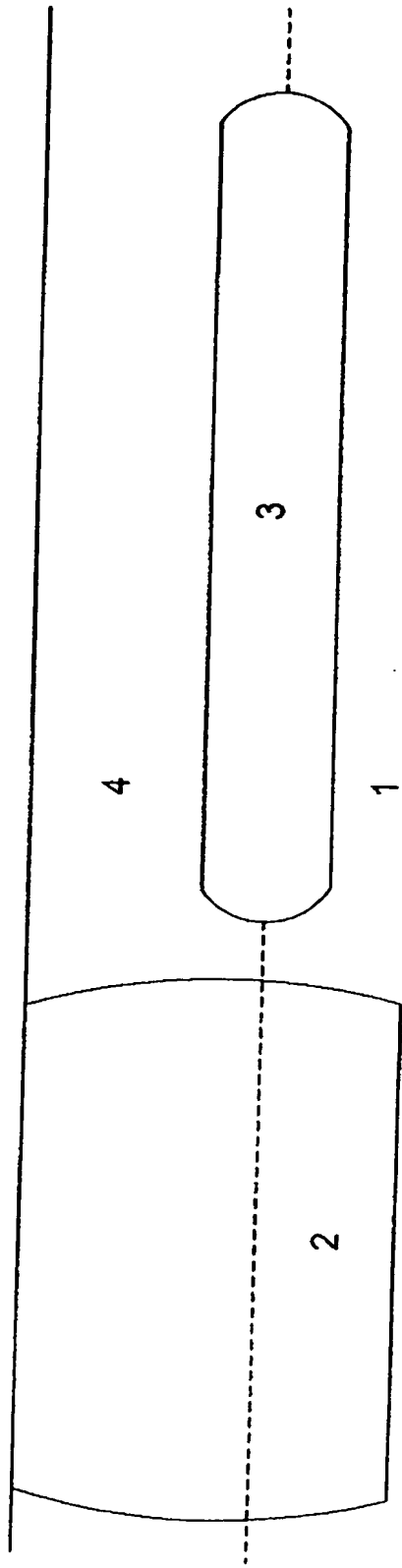


FIG 1B

vertical PNP bipolar transistor

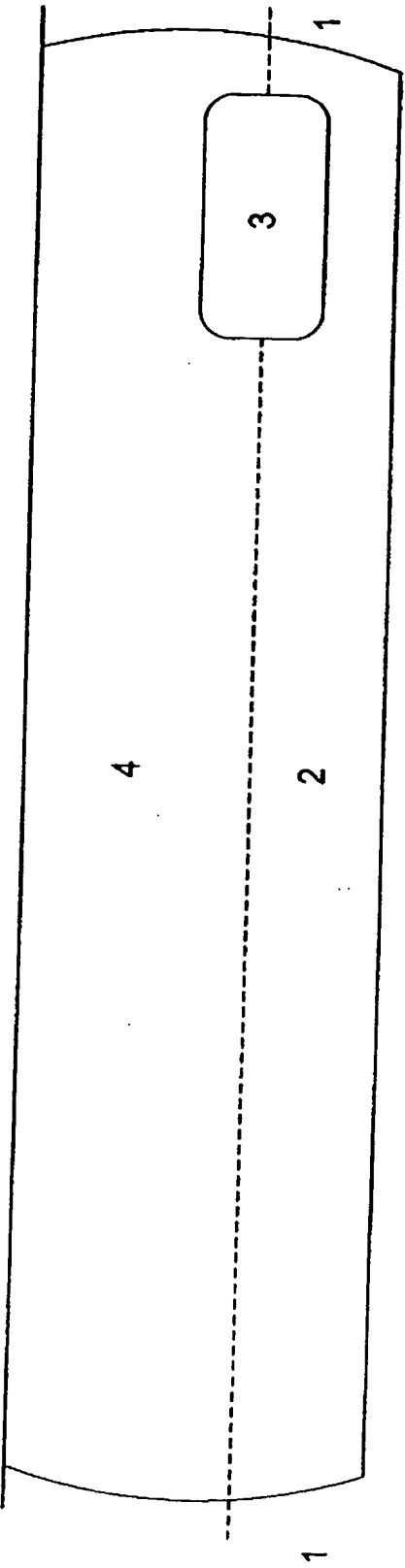
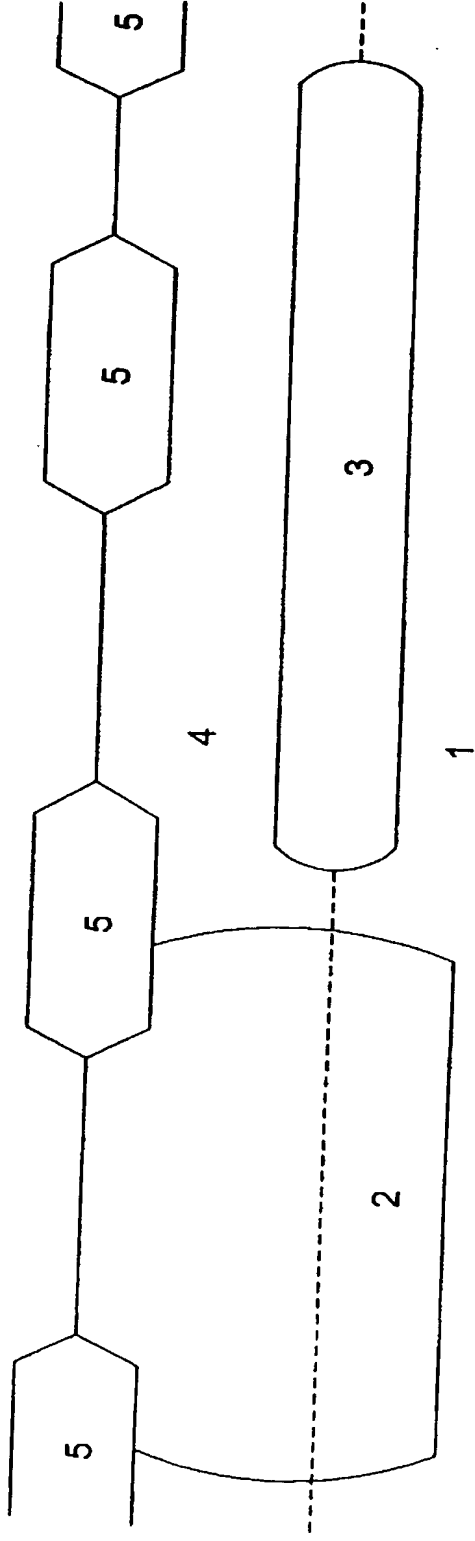


FIG 2A

NMOS transistor



NPN bipolar transistor

FIG 2B

vertical PNP bipolar transistor

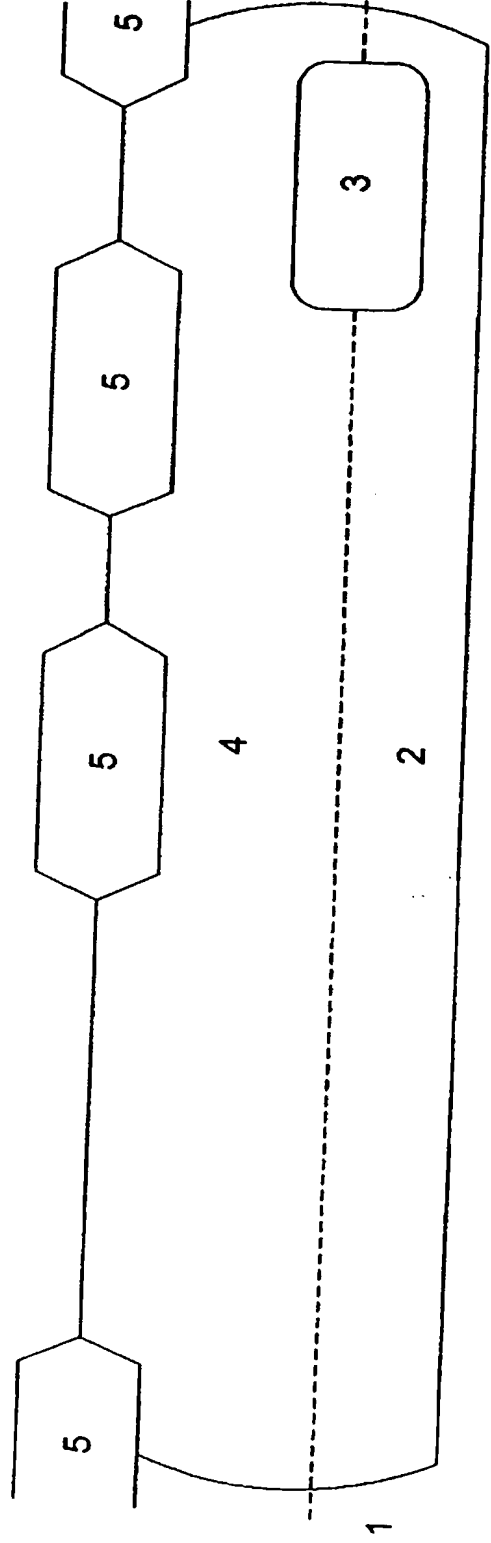
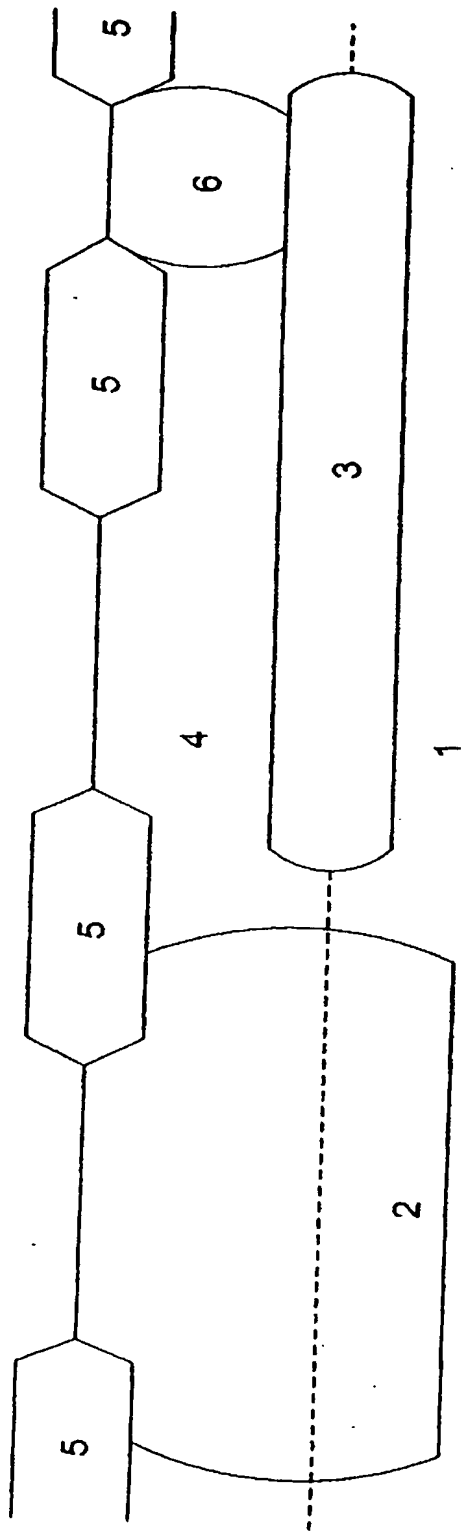


FIG 3A

NMOS transistor



NPN bipolar transistor

FIG 3B

vertical PNP bipolar transistor

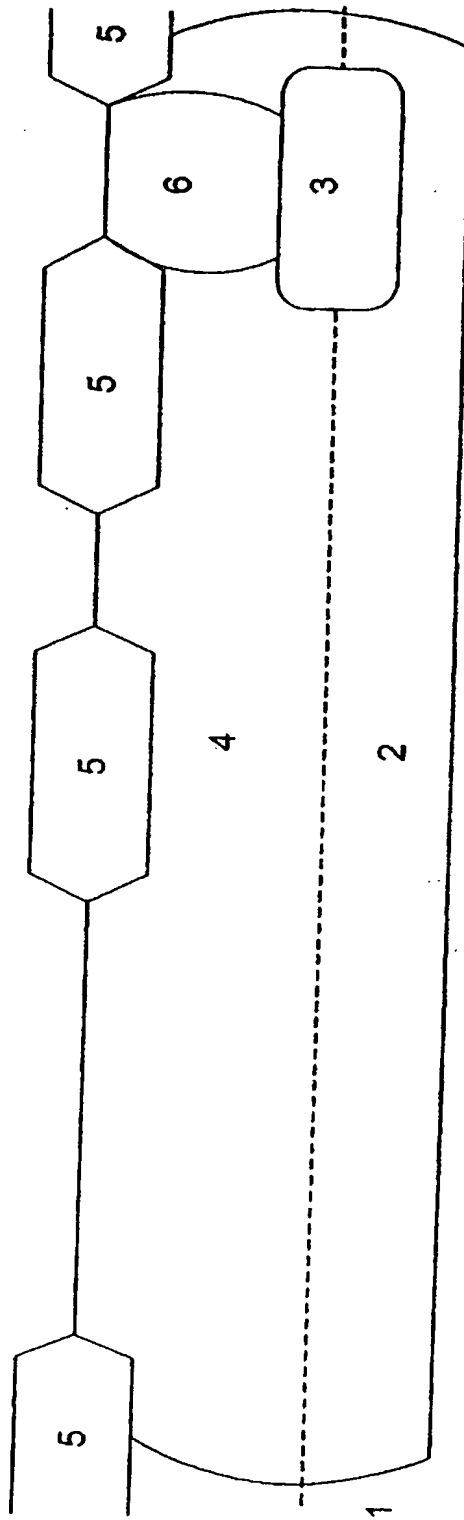


FIG 3C

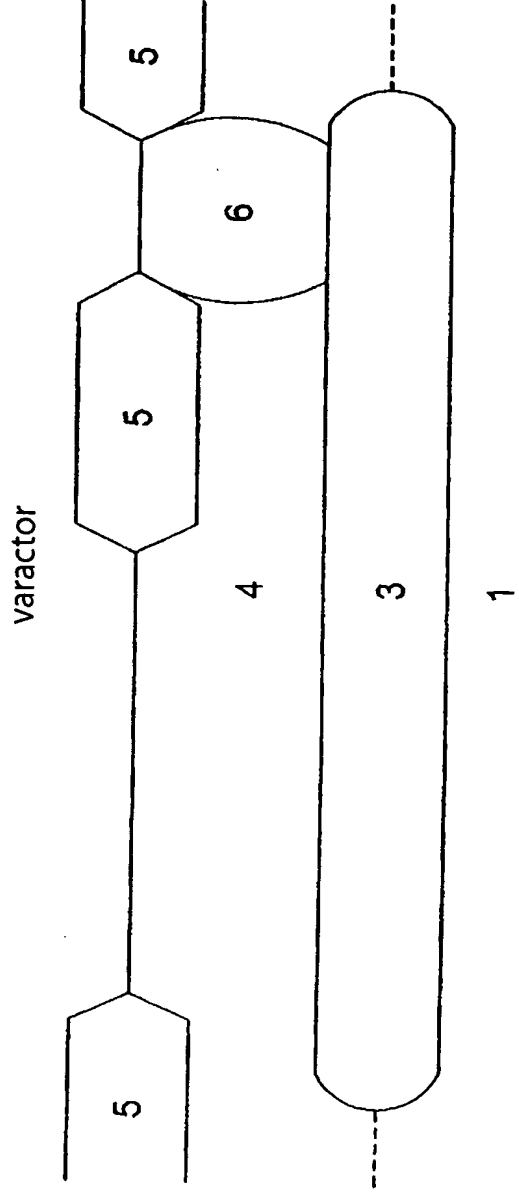
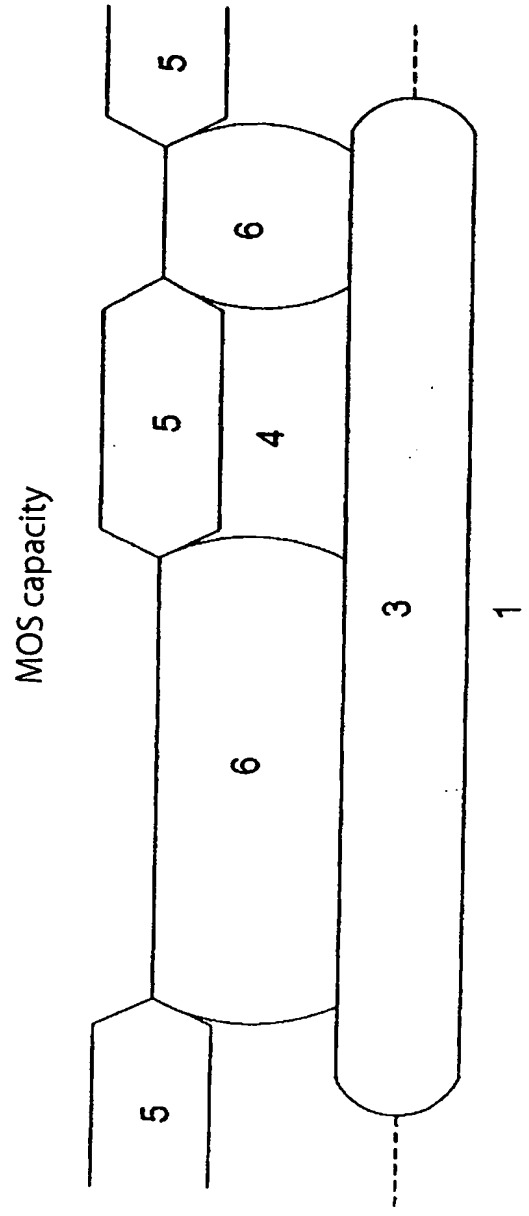
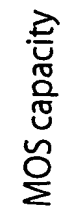


FIG 3D



MOS capacity



56F



MOS capacity



FIG 7B

NMOS transistor

NPN bipolar transistor

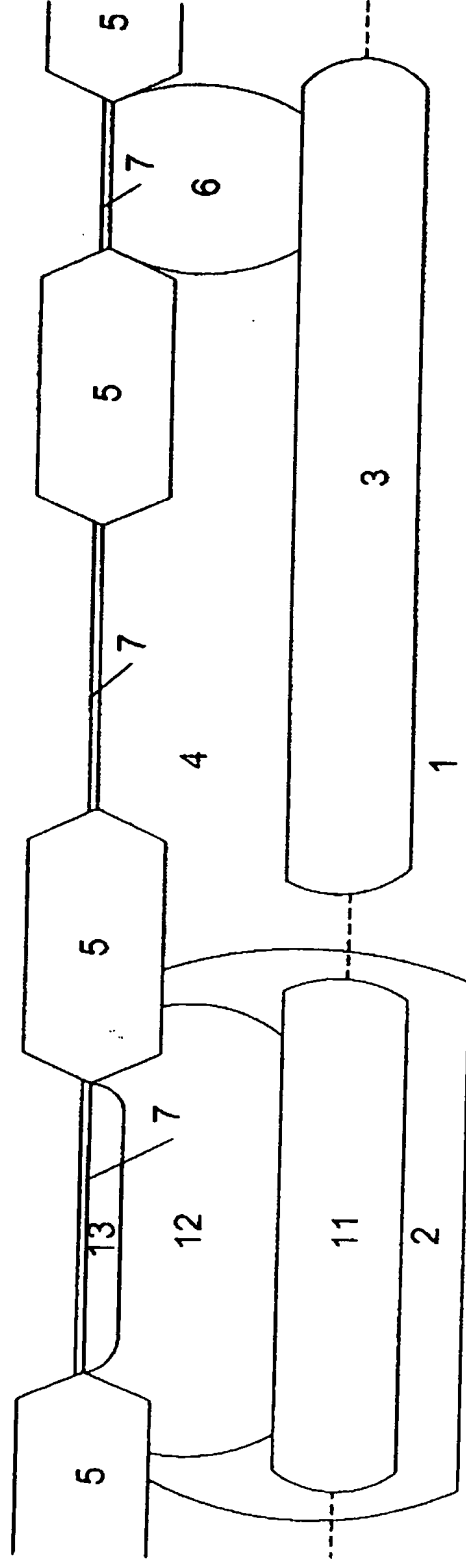


FIG 8

NMOS transistor

NPN bipolar transistor

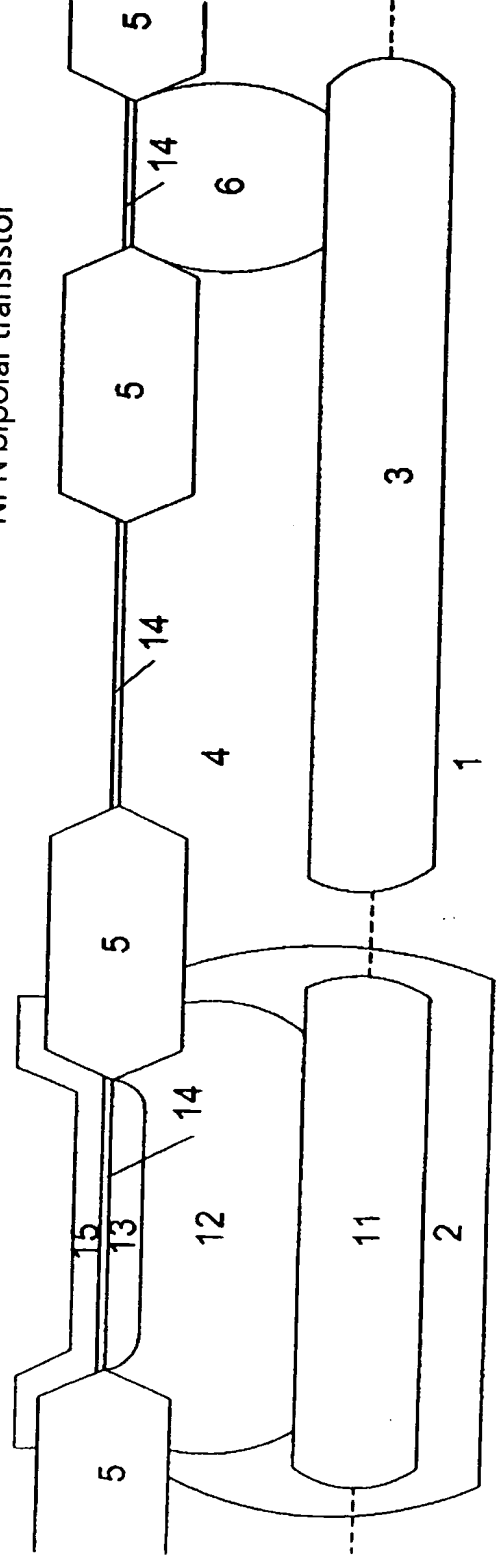


FIG 9

vertical PNP bipolar transistor

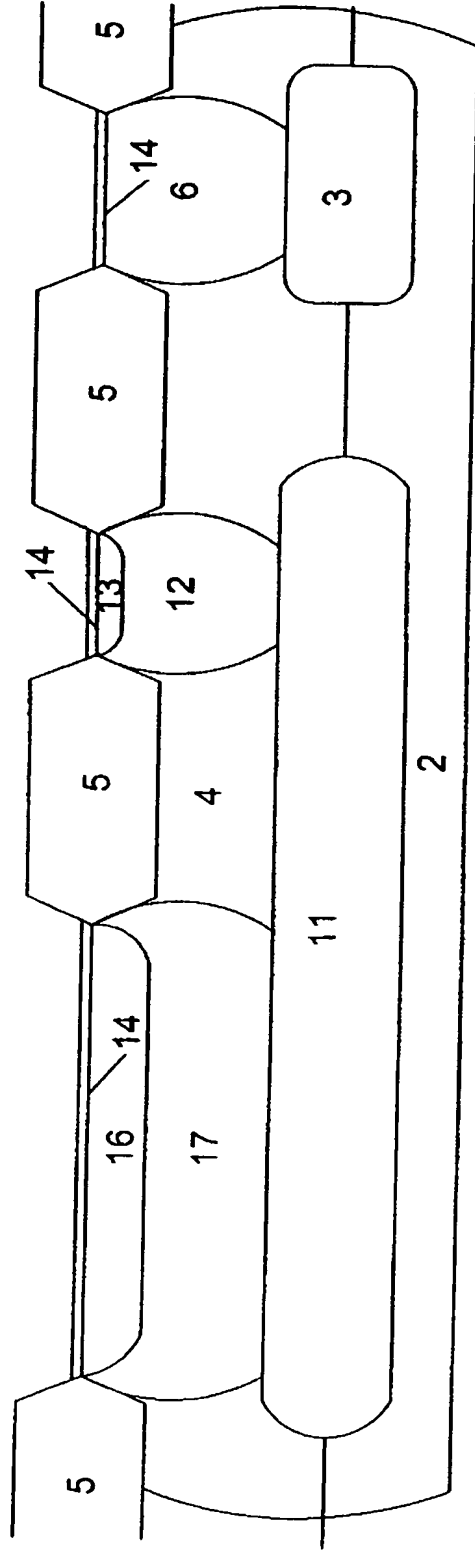
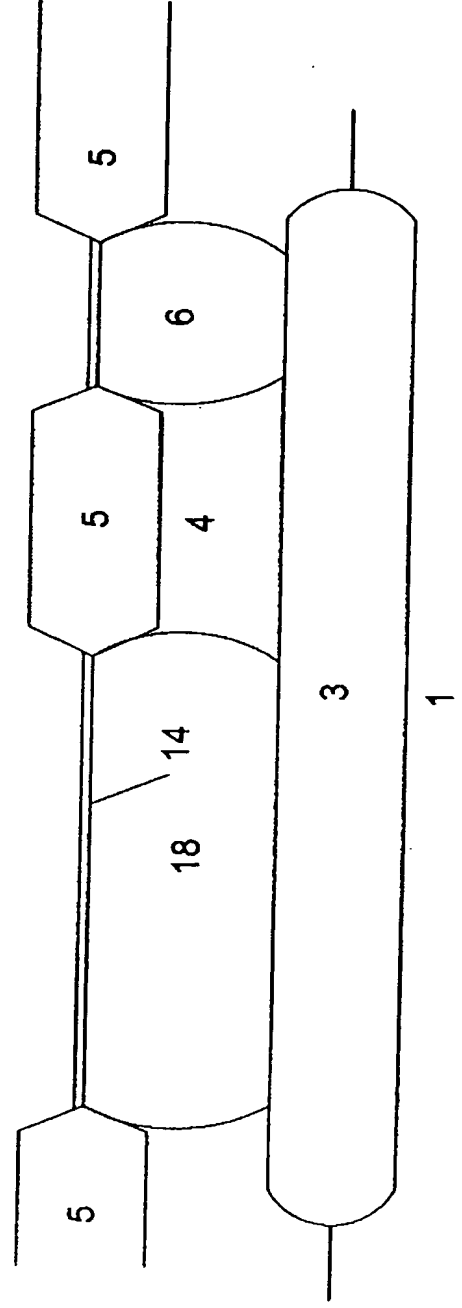


FIG 10

varactor



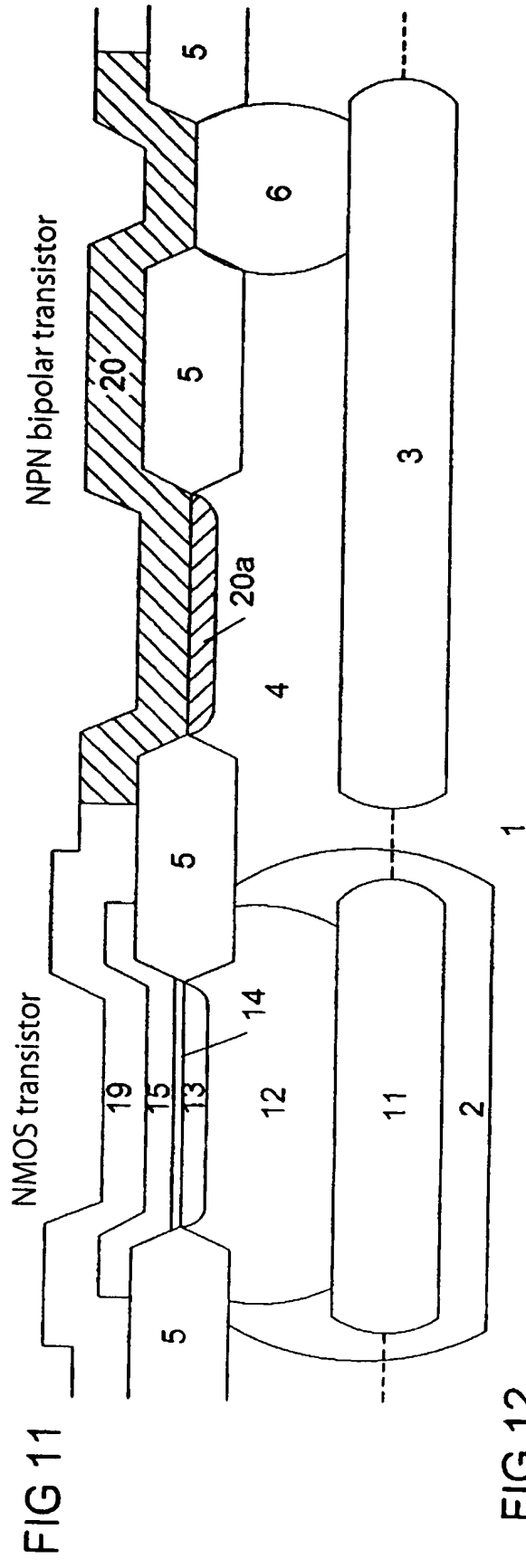
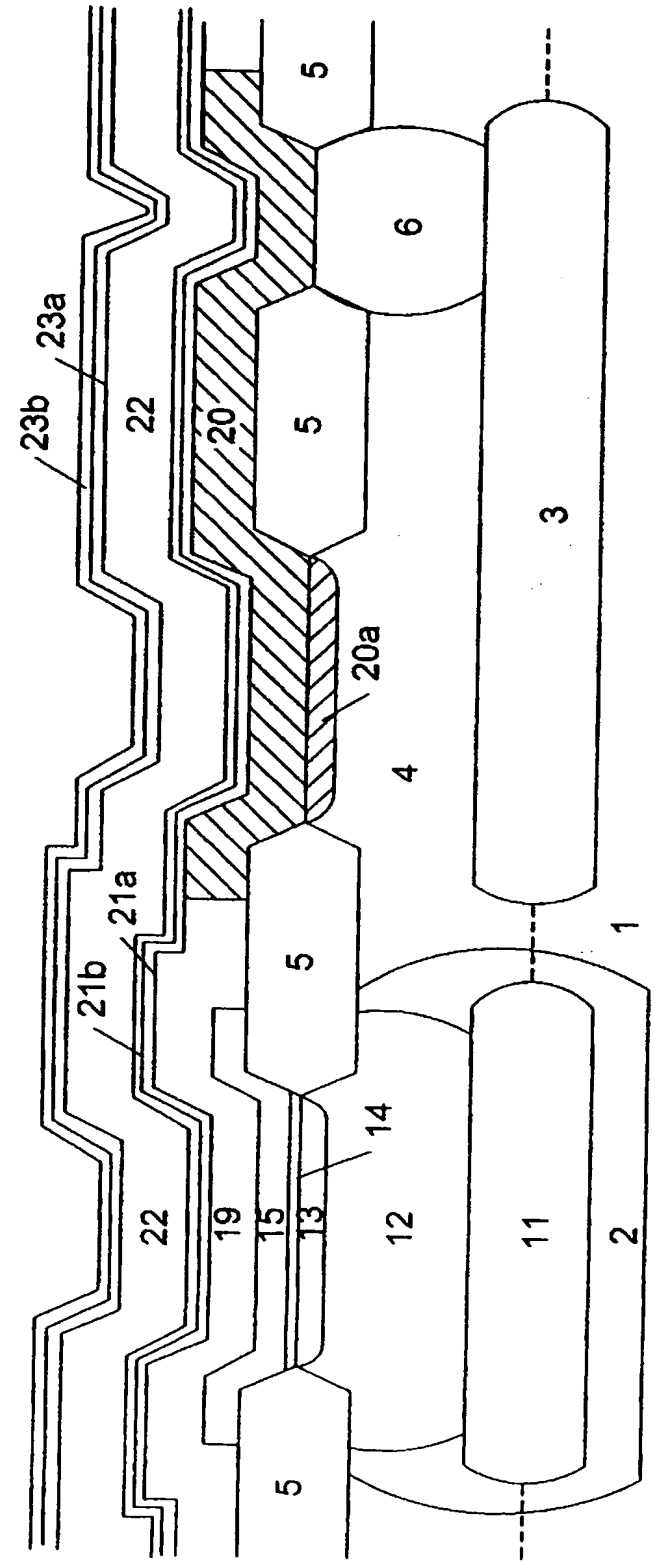


FIG 12



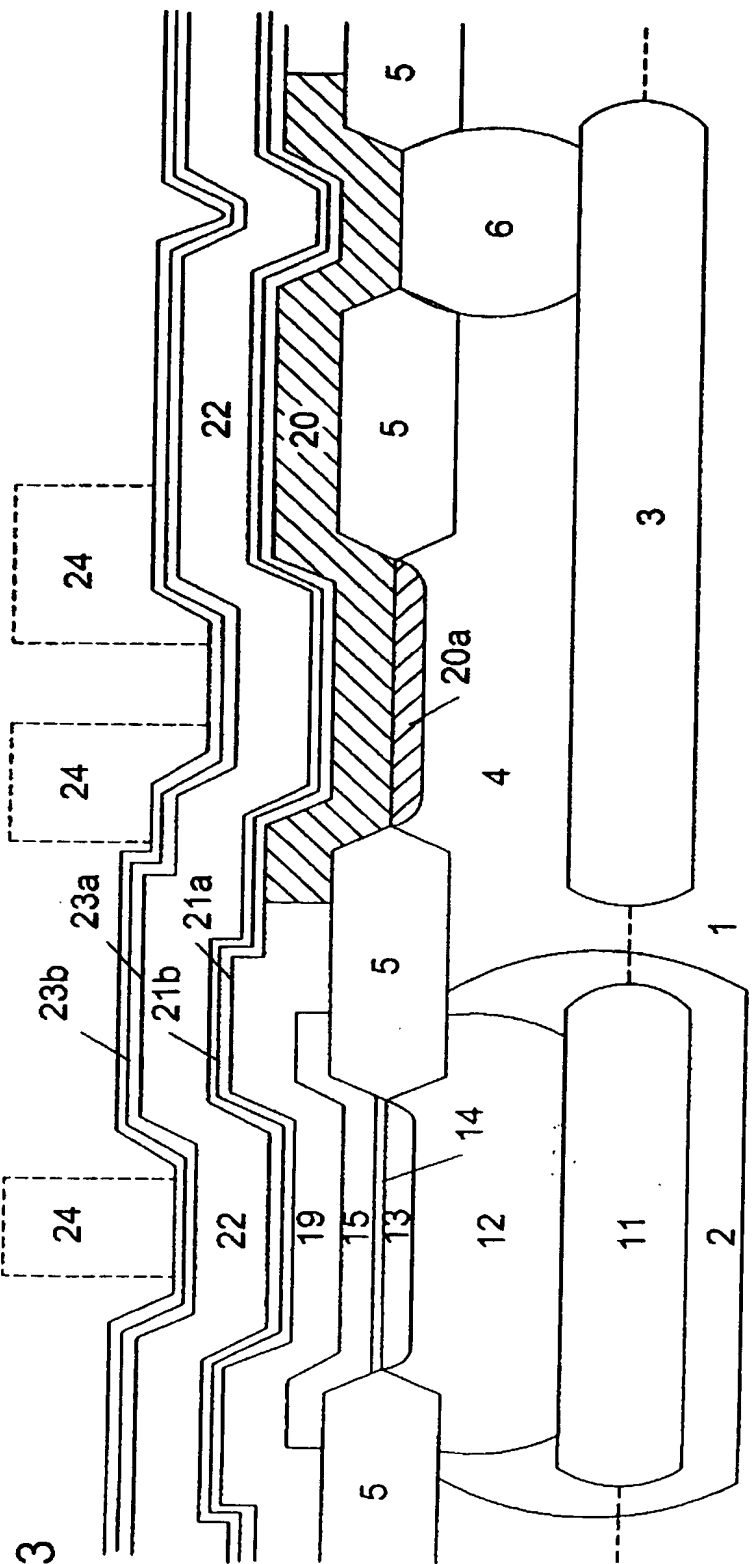
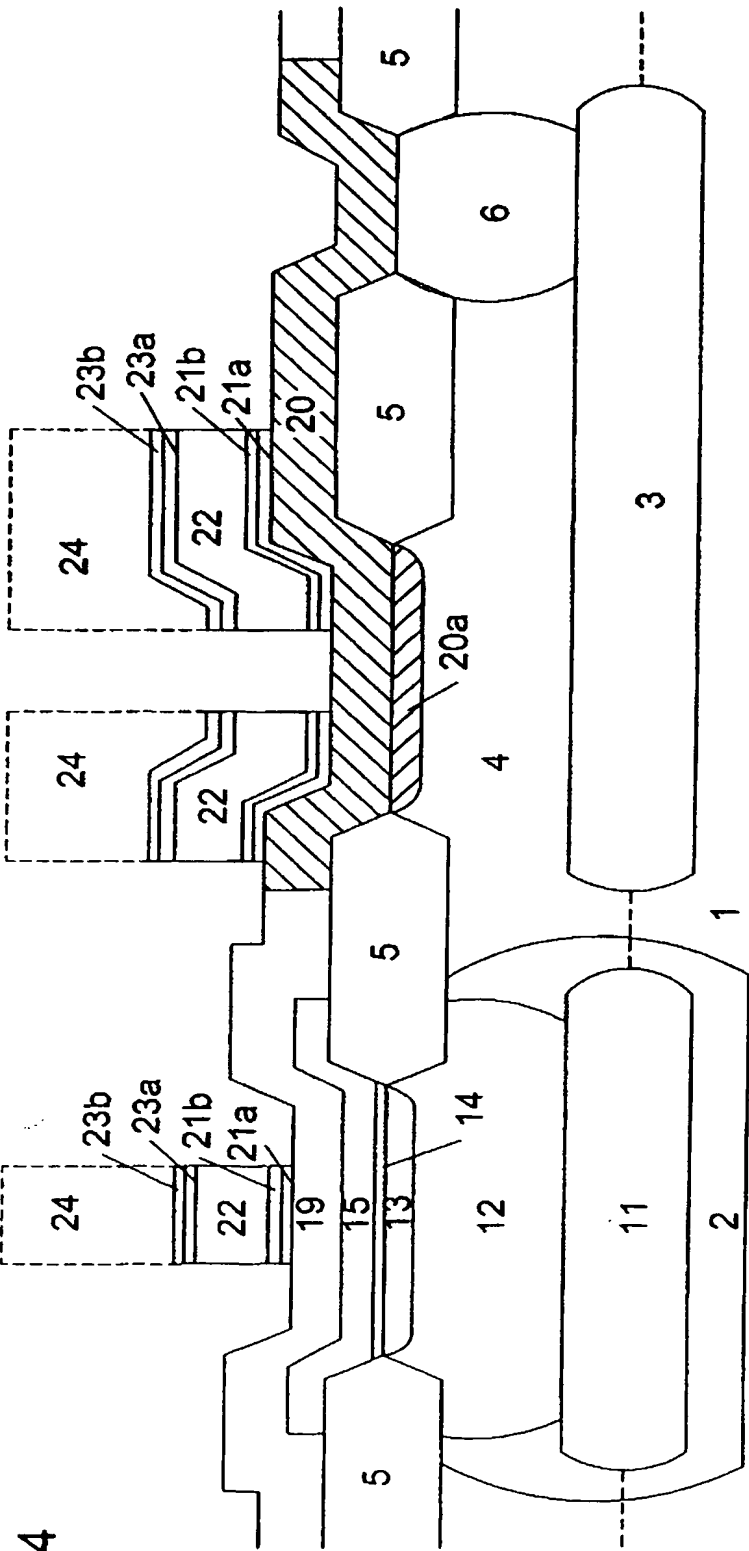


FIG 13

NMOS transistor

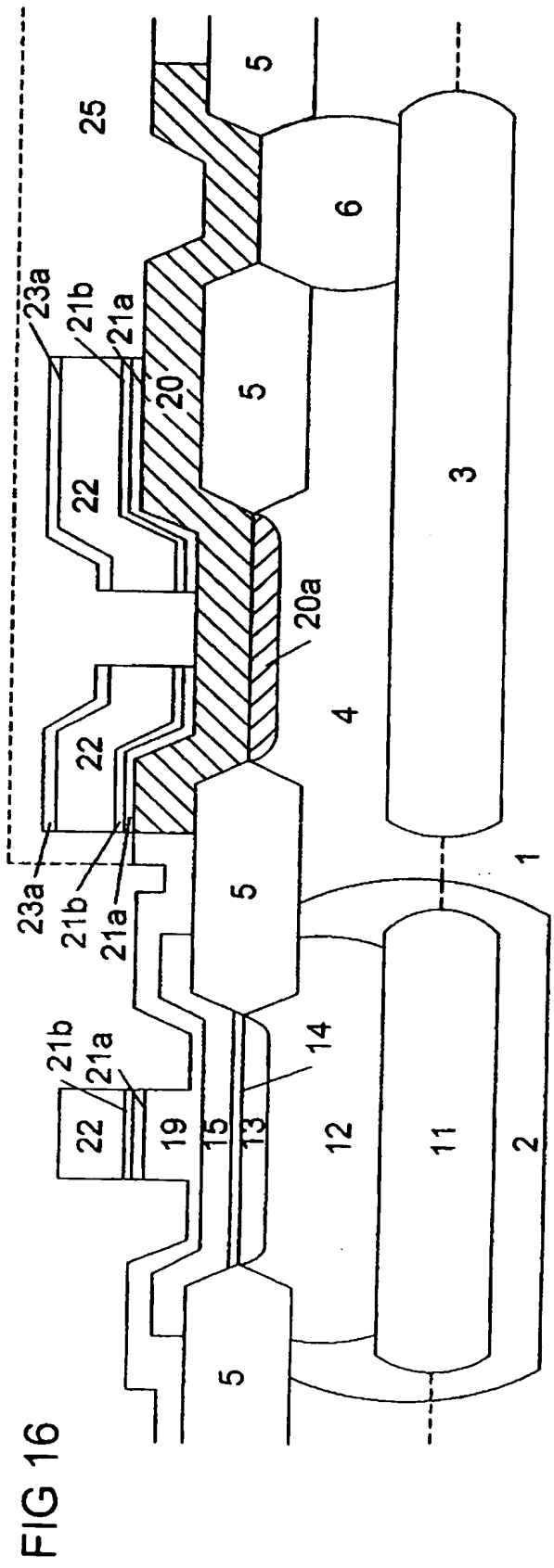
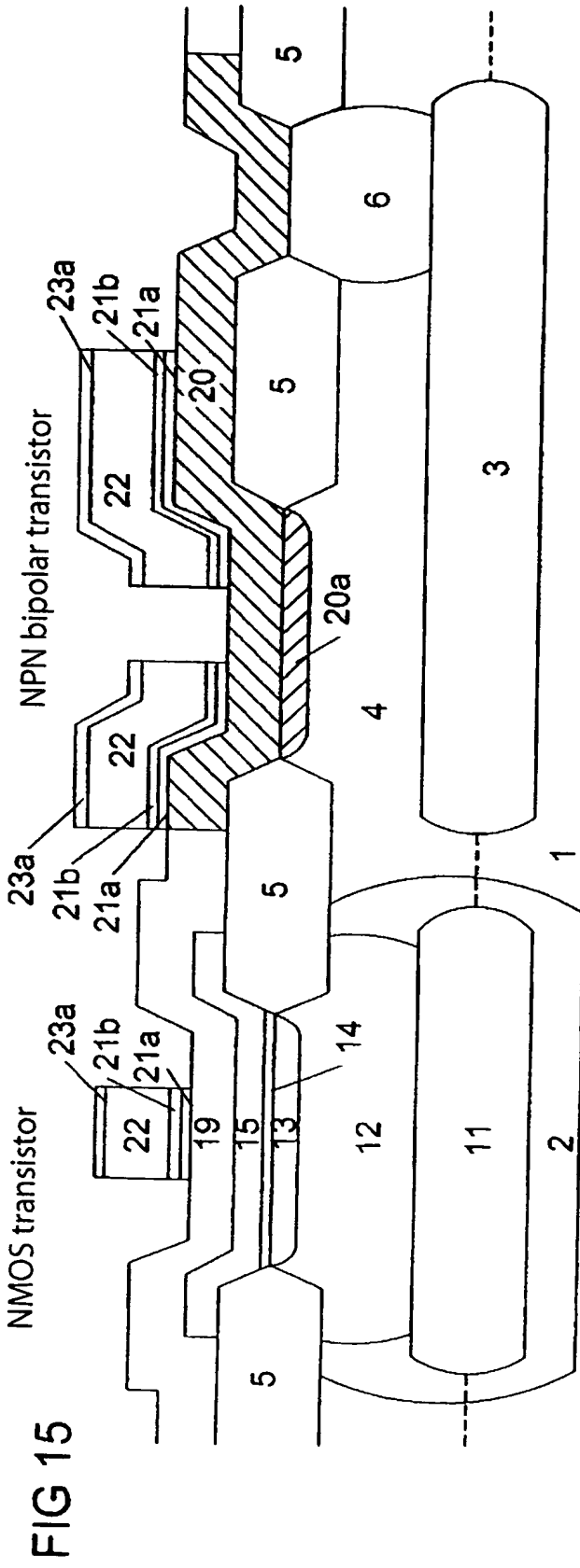
NPN bipolar transistor

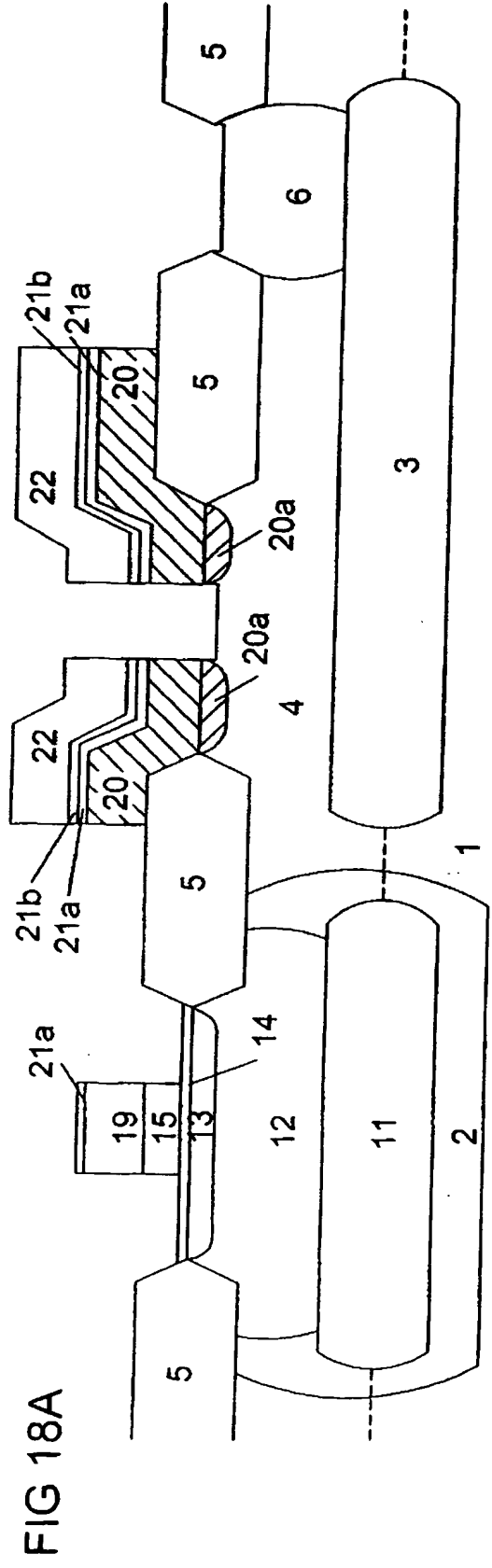
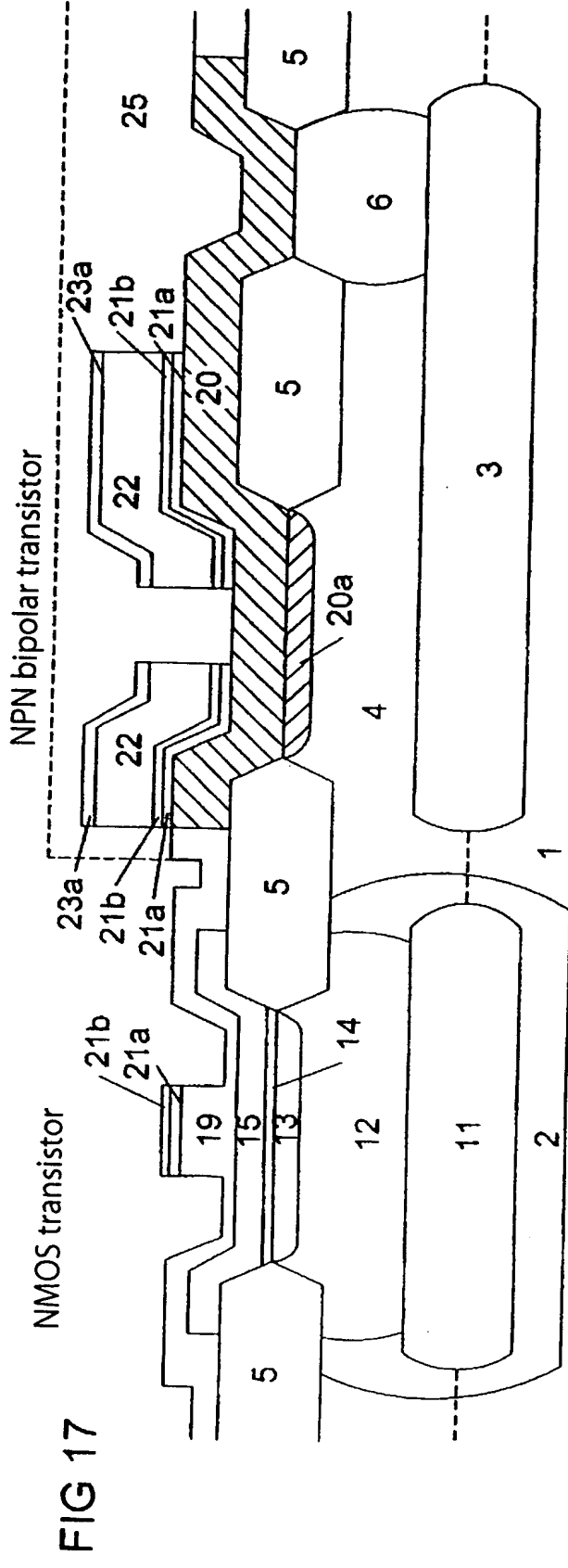


NPN bipolar transistor

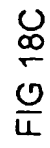
NMOS transistor

FIG 14





vertical PNP bipolar transistor



This diagram shows a cross-sectional view of a semiconductor device. On the left, a structure labeled "varactor" is shown, consisting of a stack of layers: a top layer (22), a middle layer (20), and a bottom layer (21a). A dashed line (21b) indicates the boundary between the middle and bottom layers. The varactor is positioned above a series of cells. The cells are arranged in a row, with a central cell (18) and two side cells (5). The central cell (18) is divided into two regions: a top region (20a) and a bottom region (20). The side cells (5) are also divided into two regions: a top region (5) and a bottom region (5). The entire structure is supported by a substrate (1). The top surface of the device is labeled 1, and the bottom surface is labeled 3.

FIG 18D

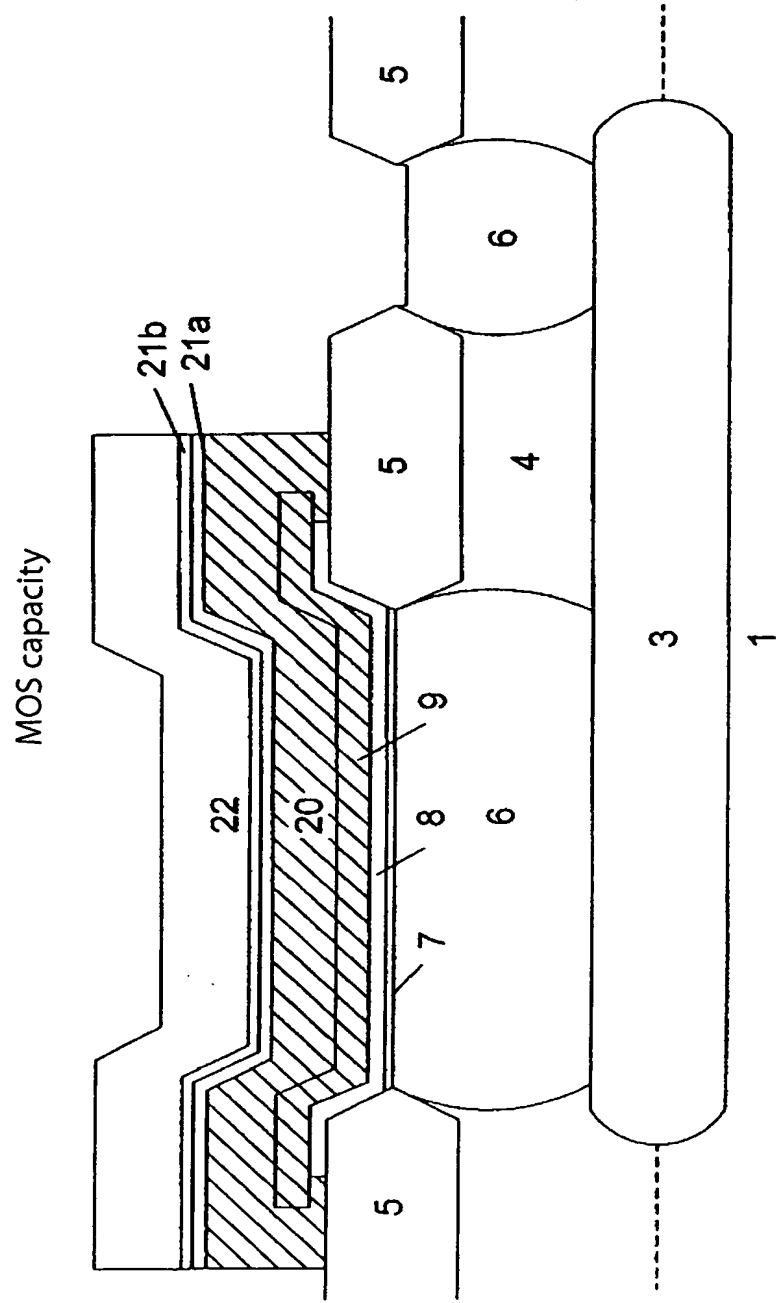


FIG 19

NMOS transistor

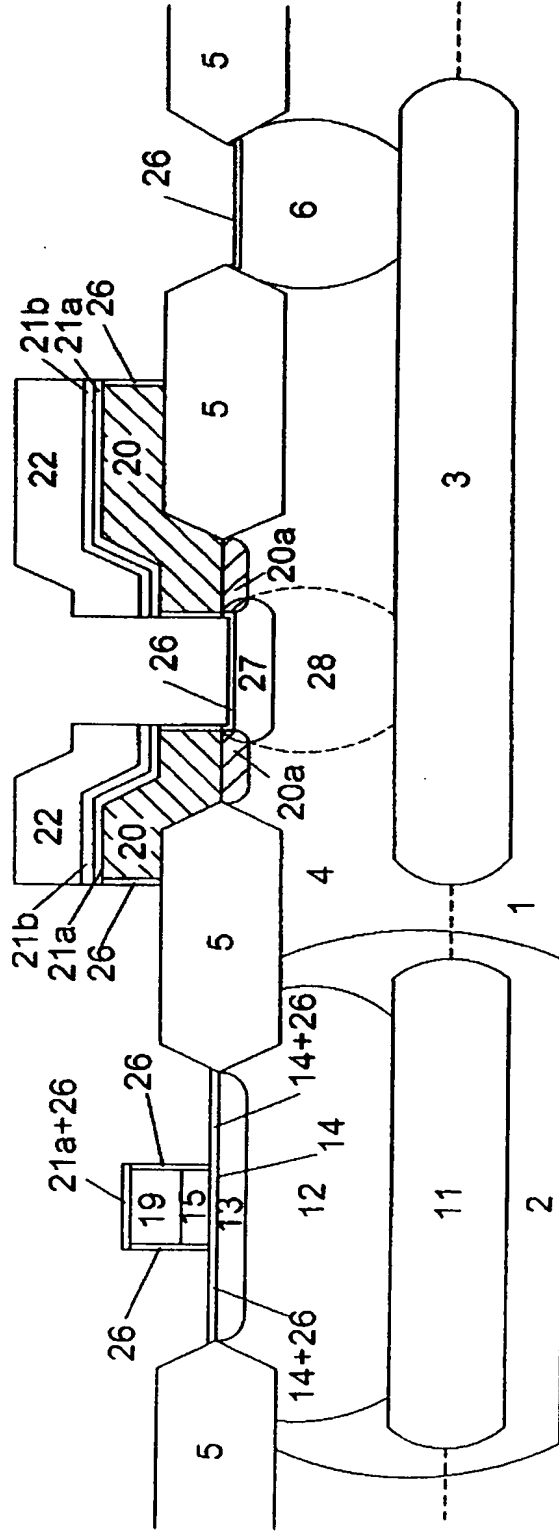


FIG 20

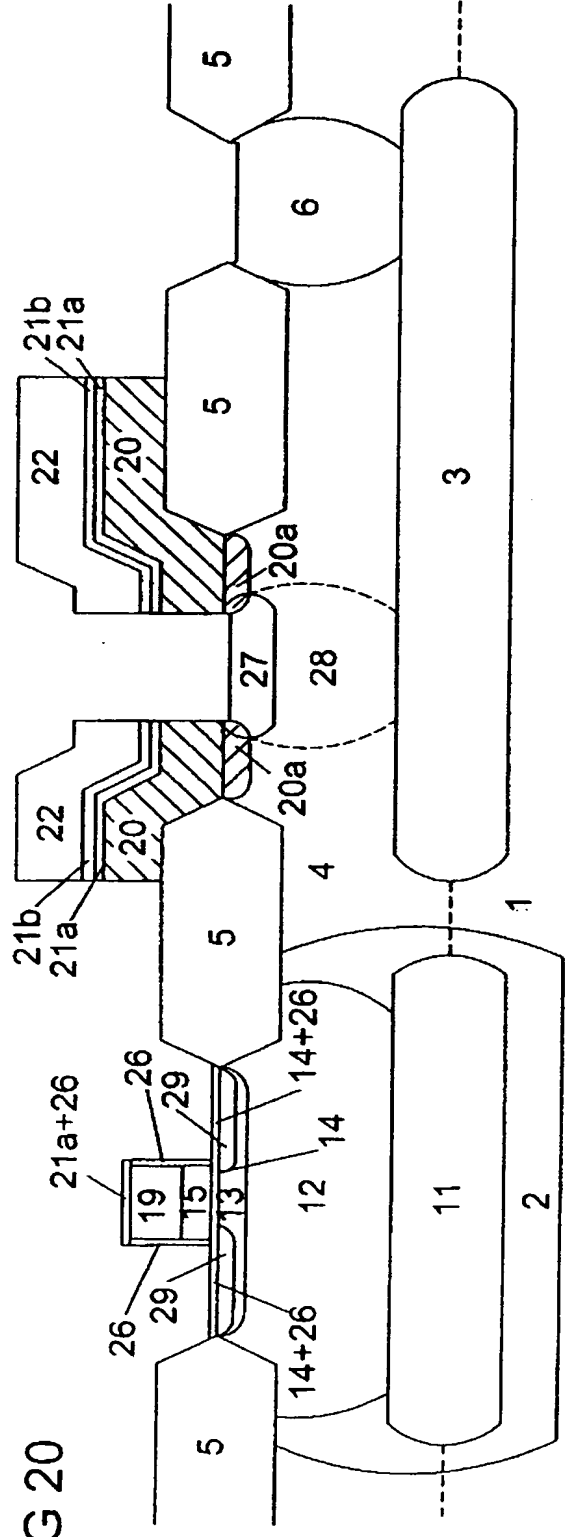


FIG 21

NMOS transistor

NPN bipolar transistor

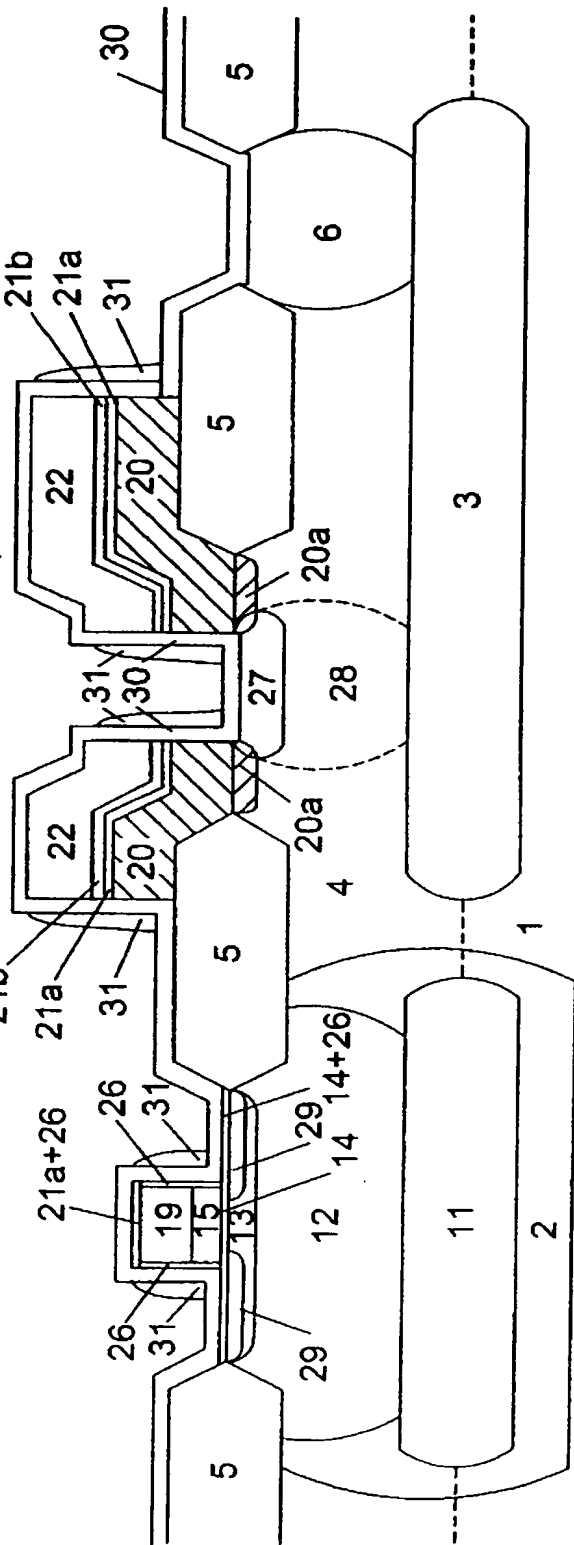
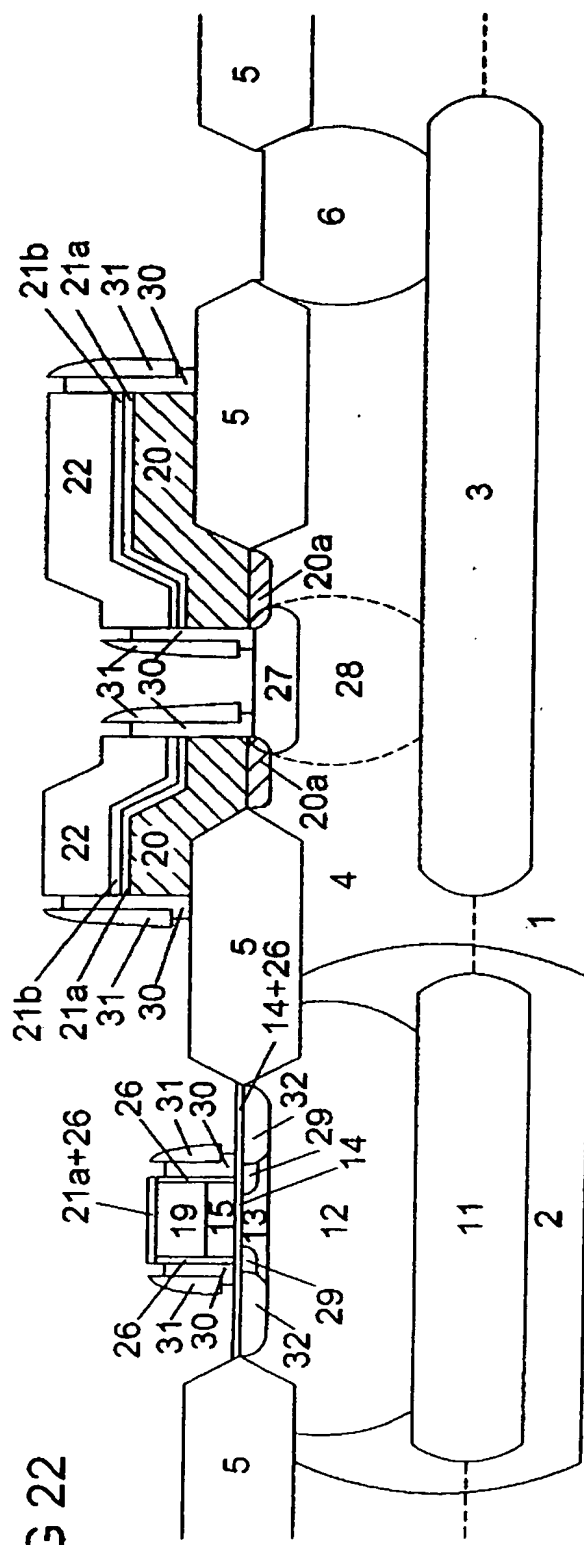


FIG 22



NPN bipolar transistor

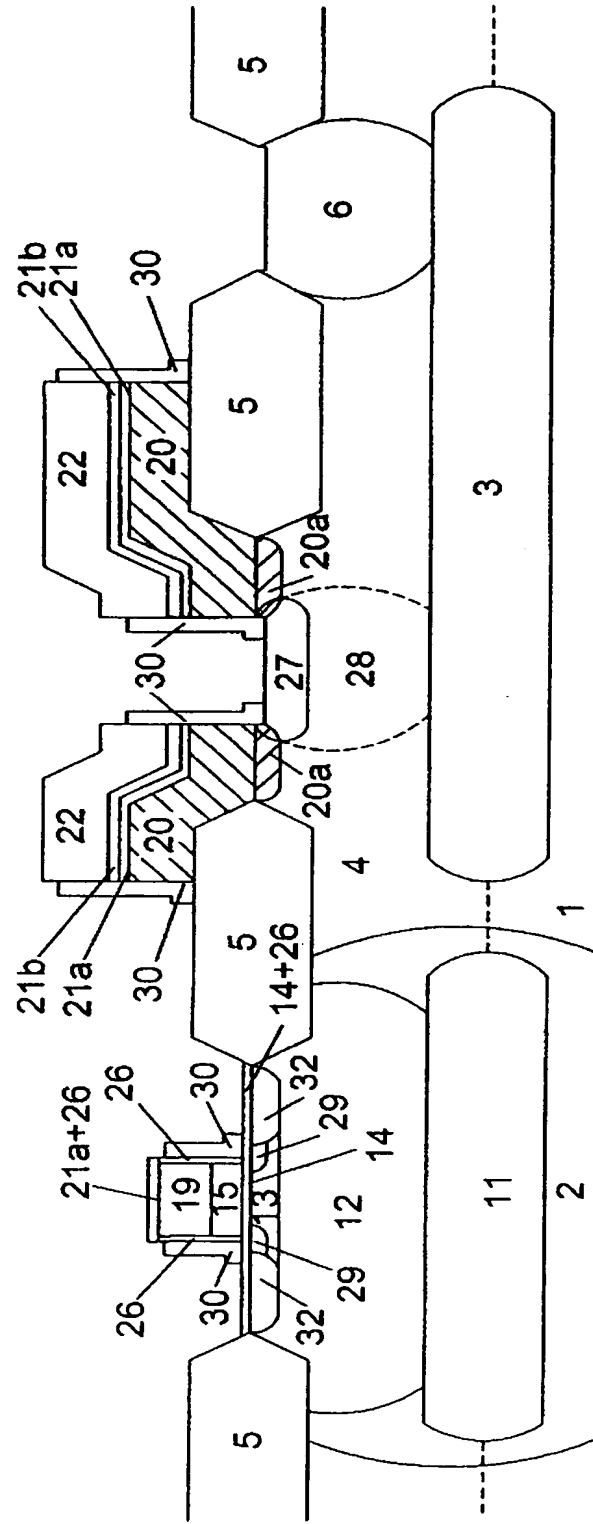


FIG 24A

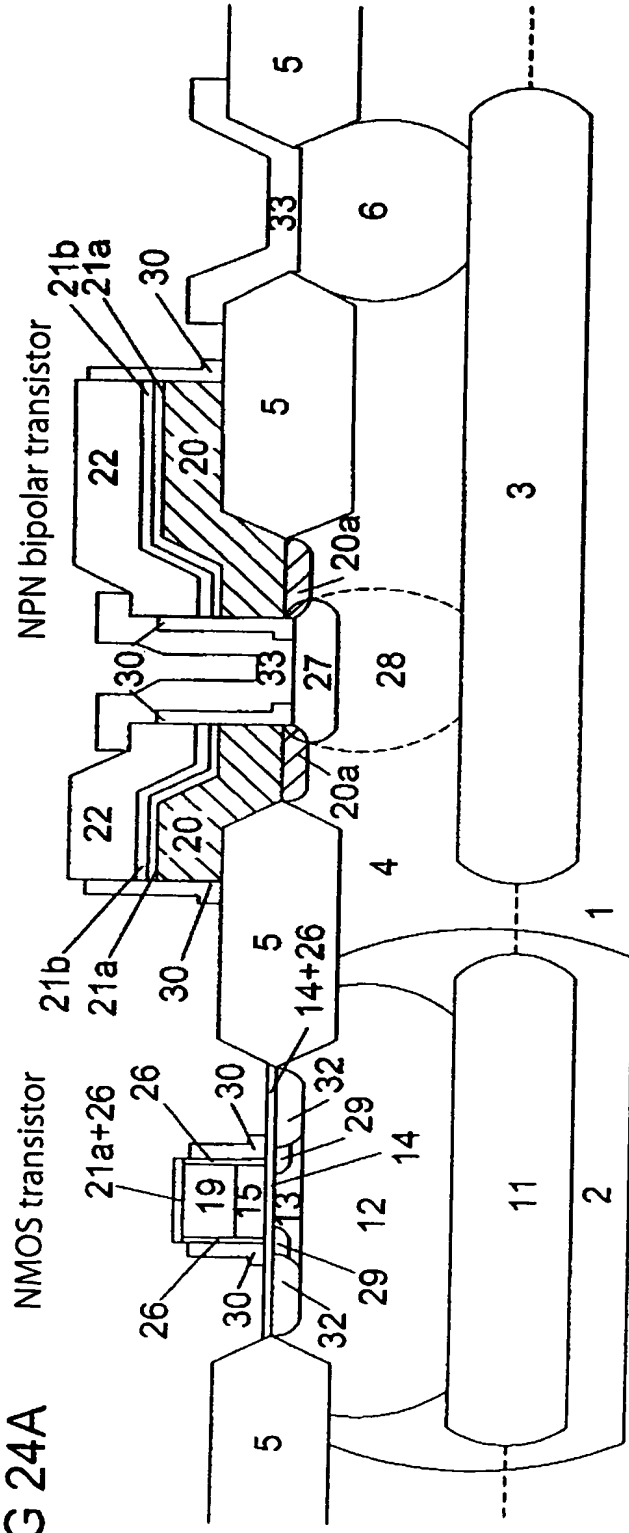


FIG 24B

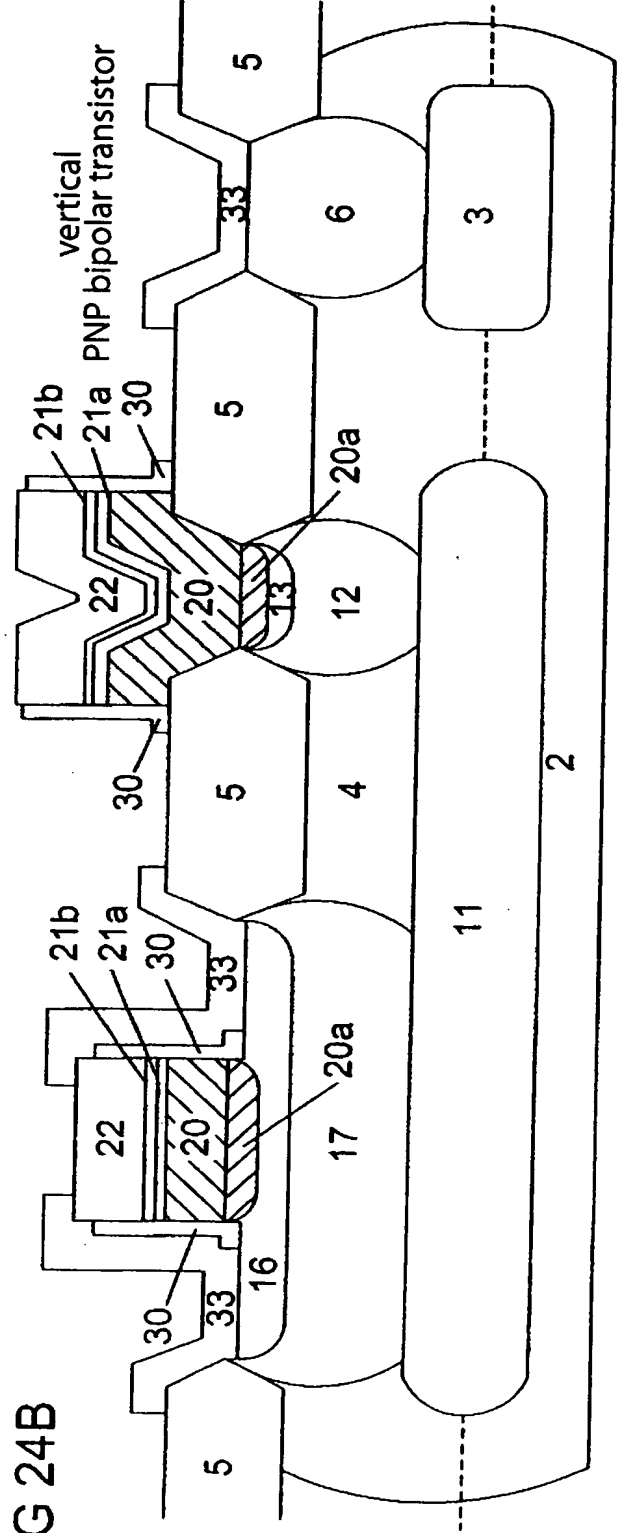


FIG 24C

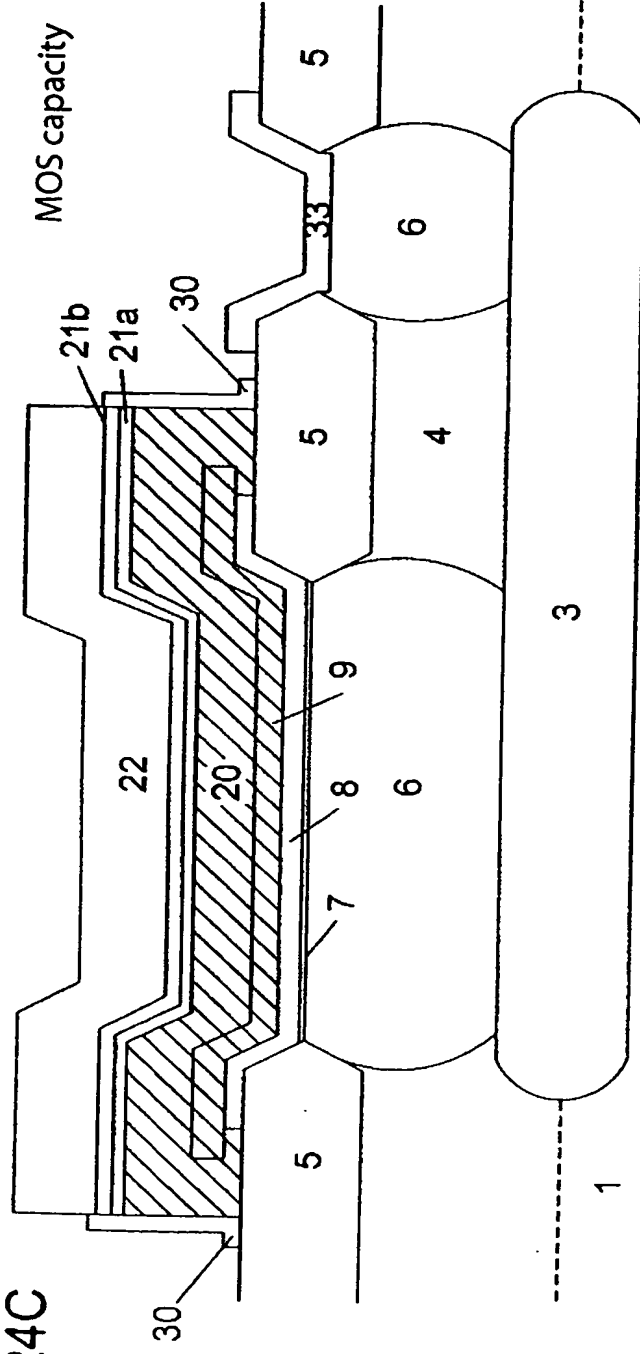


FIG 24D

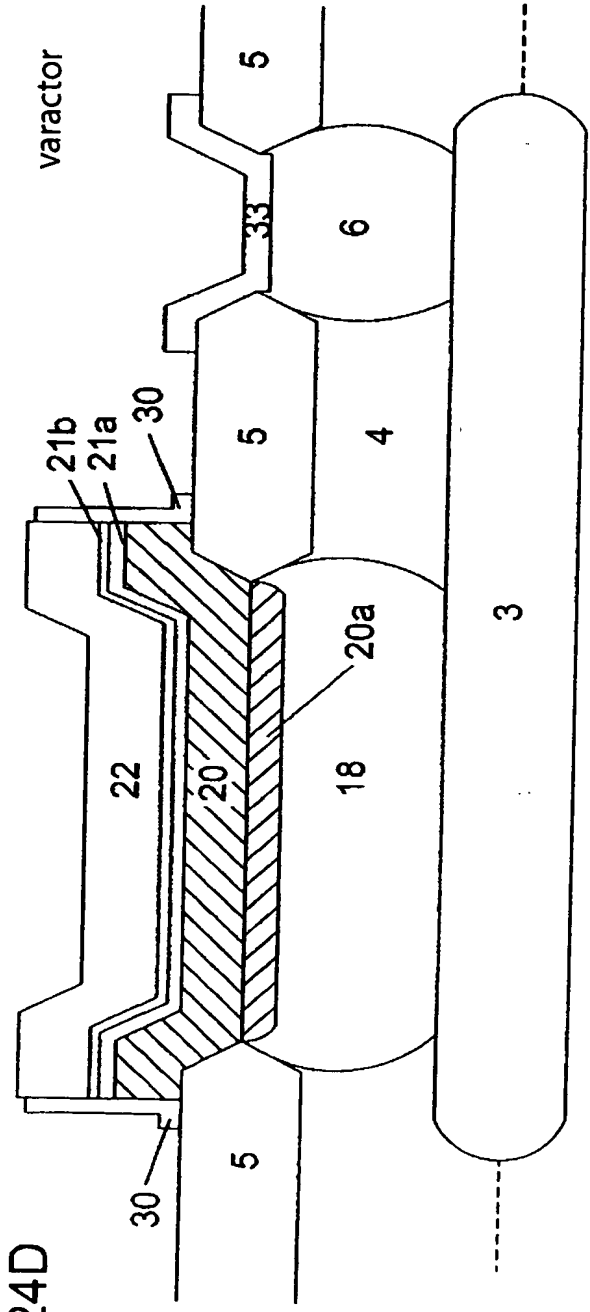


FIG 25

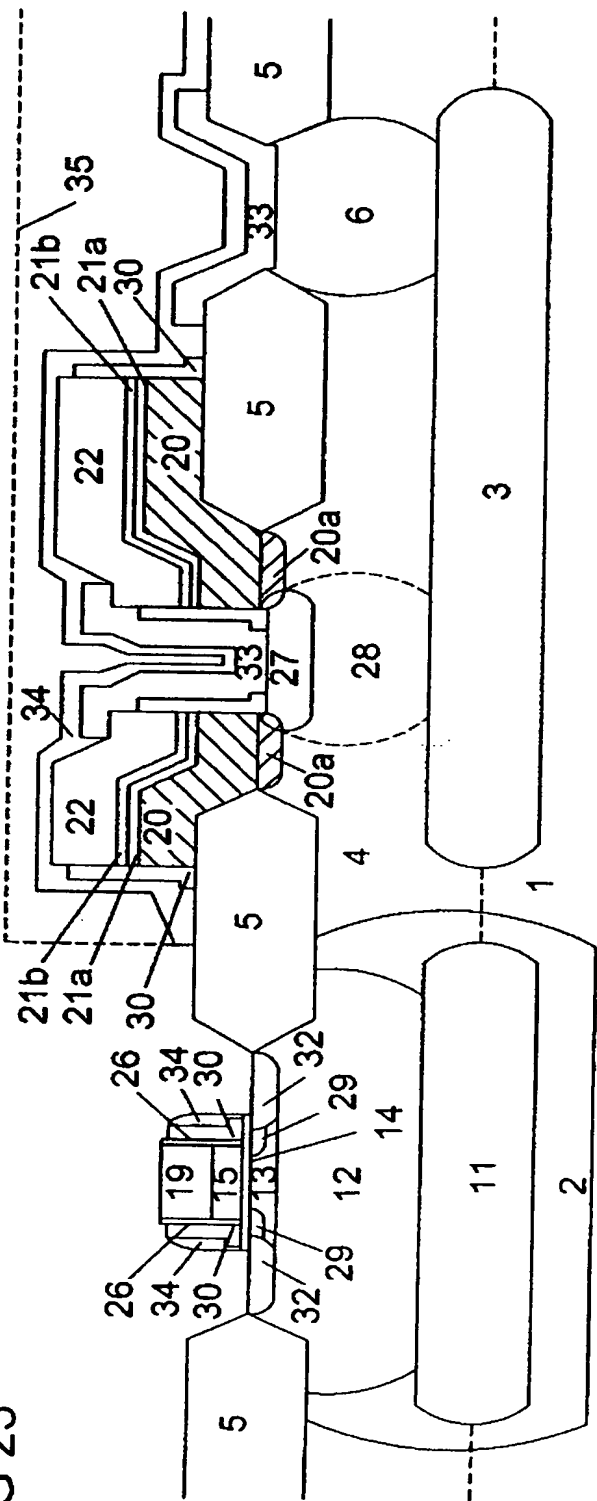


FIG 26

